Consultation Questionnaire Exemptions 15 and 15(a) of RoHS Annex III

Current wording of the exemption:

15 Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages

15(a) Lead in solders to complete a viable electrical connection between the semiconductor die and carrier within integrated circuit flip chip packages where at least one of the following criteria applies:
— a semiconductor technology node of 90 nm or larger;
— a single die of 300 mm2or larger in any semi­conductor technology node;
— stacked die packages with die of 300 mm2or larger, or silicon interposers of 300 mm2 or larger.

# Acronyms and Definitions

FCP Flip chip package

STM STMicroelectronics

# INTRODUCTION

## Background

Bio Innovation Service, UNITAR and Fraunhofer IZM have been appointed[[1]](#footnote-2) by the European Commission through for the evaluation of applications for the review of requests for new exemptions and the renewal of exemptions currently listed in Annexes III and IV of the RoHS Directive 2011/65/EU.

STM et al. submitted a request[[2]](#footnote-3) for the renewal of the above-mentioned exemption. The request has been subject to a first completeness and plausibility check. The applicant has been re-quested to answer additional questions and to provide additional information, available on the request webpage of the stakeholder consultation.[[3]](#footnote-4)

The stakeholder consultation is part of the review process for the request at hand. The objective of this consultation and the review process is to collect and to evaluate information and evidence according to the criteria listed in Art. 5(1)(a) of Directive 2011/65/EU.[[4]](#footnote-5)

To contribute to this stakeholder consultation, please answer the below questions until the 27th of May 2020.

## Summary of the Exemption Request

Solder bumps are minute solder spheres (typically ~80um in diameter) connecting a Silicon (or other semiconductor) die with a carrier in flip chip Application Specific Integrated Circuit (ASIC) packages. The bump solder joint is extremely sensitive: stress resulting from the large mismatch in the coefficient of thermal expansion (CTE) between the silicon (or other semiconductor) die and the carrier is concentrated at the small bump interface area and transferred by the bump to the fragile low-K dielectric layers inside the Semiconductor die. In addition, the hair- thin solder connection itself needs to withstand these high stresses.

Lead- containing solder materials are softer and more ductile than lead- free solders. They have a better ability to absorb stresses resulting from CTE mismatch between semiconductor and carrier and transfer less stress to the low-K dielectric layers. In addition, they can better withstand stress and are less prone to solder cracking. Leaded solders can provide a lower melting temperature, thus require lower processing temperature creating less package stress. The use of leaded solders helps resolve failures such as cracks in low- K dielectric layers, solder cracks, silicon cracks, delamination and package warpage.Older flip chip product technologies, flip chip products with large die and large interposers for stacked die, are not able to meet long-term reliability requirements with lead-free solder bumps on the die. Older product technologies are defined as those having transistor gate lengths of 90nm and longer. Large die and large interposers are defined as being 300mm2 (300 mm2 for monolithic die and large interposers) or larger.

Flip chips are commonly used in long life, high reliability applications that remain in the field for over 20 years and require continuous availability as replacement parts. Legacy flip chip devices and many large die devices are older products that have declining volume year-on-year making it difficult to justify an all-layer and material redesign (this is usually not technically possible, as described in this renewal request). Removing these products from the market would create long supply gaps with minimal impact on the amount of lead in the EU market, but prevent the sale of many types of products in the EU.

Silicon technology nodes with transistor gate lengths longer than 250 nm used aluminum interconnect in the wafer processing backend. Later on, industry had to migrate to copper interconnect due to device performance expectations and increased circuit densities. Devices on the 250nm to 90nm technology nodes converted to a common low dielectric constant film (low-k): fluorinated tetraethyl orthosilicate (F-TEOS). F-TEOS made copper interconnect possible. At the time, F-TEOS was a breakthrough in materials engineering and from an electrical perspective it reduced capacitance in the silicon wafer backend dielectric stack. Reducing the resistance of interconnect wiring and reducing the capacitance of the interlayer dielectric (ILD) allow for higher device clock speeds. Dielectric capacitance was significantly reduced with F-TEOS when compared to the dielectrics used earlier in the semiconductor industry. The porous nature of the film is what reduces the capacitance and F-TEOS offered improved electrical performance at the expense of film mechanical strength.

The low mechanical strength of F-TEOS makes it susceptible to dielectric fracturing beneath the under bump metallization (UBM) on the silicon chip (die) with lead-free wafer bumps, due to the increased stresses imposed. This does not occur with leaded C4 (controlled collapse chip connection) wafer bumps. Lead-free wafer bumps are significantly less ductile than those containing lead, and the observed failure mode mechanism is driven by coefficient of thermal expansion mismatch between the silicon die and the carrier which transfers the strain to the less ductile lead-free bump and the fragile F-TEOS dielectric. Fracturing of the dielectric with Pb-free wafer bumps is commonly referred to as “ghost” or“white” bumps due to the way they appear by acoustic imaging. Not only can the failure mode reduce assembly yields, it can also adversely impact product reliability.The failure may not be caught when a unit goes through component assembly and final testing. Compromised units that ship are at high risk of failing during the customer’s board level assembly processor in the field. The failure rates are unacceptably high. This failure mode does not occur with wafer bumps that contain lead because leaded bumps absorb the stress associated with the coefficient of thermal expansion mismatch between the silicon chip and the substrate to which the solder attaches.

# Questions

1. STM et al. requested the renewal2 of the above exemptions with the following wording for the maximum validity periods of 5 years for cat. 1-7 and 10 and for 7 years for cat. 8 and 9:



* 1. Please let us know whether you support or disagree with the wording, scope and requested duration of the exemption. To support your views, please provide detailed technical argumentation / evidence in line with the criteria4 in Art. 5(1)(a).
	2. If applicable, please suggest an alternative wording and duration and explain your proposal.
1. Please provide information concerning possible substitutes or elimination possibilities at present or in the future so that the requested exemption could be restricted or revoked. In particular please let us know whether the proposed criteria as to the 300 mm² die size in association with the technology nodes still reflect the current state of science and technology of lead substitution or elimination. Further, it would be important to understand whether the replacement of silicon by plastics interposers in modern FCPs makes the respective part of the above exemption 15(b) dispensable.
Note: The redesign of “old” design FCPs is not in the scope of this question. We therefore ask you to relate your answers to modern design FCPs that were from the beginning designed to accommodate the needs of lead-free solders to understand the state of science and technology.
	1. Please explain substitution and elimination possibilities and for which part of the ap-plications in the scope of the requested exemption they are relevant.
	2. Please provide information as to research to find alternatives that do not rely on the exemption under review (substitution or elimination), and which may cover part or all of the applications in the scope of the exemption request.
	3. Please provide a roadmap of such on-going substitution/elimination and research (phases that are to be carried out), detailing the current status as well as the estimated time needed for further stages.
2. Are you aware of any EEE of category 11 that require the use of exemptions 15 or 15(a)?
3. Do you know of other manufacturers producing devices of comparable features and performance like the ones in the scope of this exemption request that do not depend on RoHS-restricted substances, or use smaller amounts of these substances compared to the applications in the scope of this exemption?
4. As part of the evaluation, socio-economic impacts shall also be compiled and evaluated. For this purpose, if you have information on socioeconomic aspects, please provide details in respect of the following:
	1. What are the volumes of EEE in the scope of the requested exemptions which are placed on the market per year?
	2. What are the volumes of additional waste to be generated should the requested ex-emption not be renewed or not be renewed for the requested duration?
	3. What are estimated impacts on employment in total, in the EU and outside the EU, should the requested exemption not be renewed or be renewed for less than the re-quested time period? Please detail the main sectors in which possible impacts are expected – manufacturers of equipment in the scope of the exemption, suppliers, re-tail, users of MRI devices, etc.
	4. Please estimate additional costs associated should the requested exemption not be renewed, and how this is divided between various sectors (e.g. private, public, industry: manufacturers, suppliers, retailers).
5. Any additional information which you would like to provide?

**Please note that answers to these questions can be published in the stakeholder consultation, which is part of the evaluation of this request. If your answers contain confidential information, please provide a version that can be made public along with a confidential version, in which proprietary information is clearly marked.**

**Please do not forget to provide your contact details (Name, Organisation, e-mail and phone number) so that the project team can contact you in case there are questions concerning your contribution.**

**It would be help the review process if you could kindly provide the information in formats that allow copying text, figures and tables to be included into the review report.**

1. It is implemented through the specific contract 070201/2020/832829/ENV.B.3 under the Framework contract ENV.B.3/FRA/2019/0017 [↑](#footnote-ref-2)
2. Exemption request available at [http://www.rohs.biois.eu/15\_15(a)\_Exemption%20Request%20\_16012020\_final.pdf](http://www.rohs.biois.eu/15_15%28a%29_Exemption%20Request%20_16012020_final.pdf) [↑](#footnote-ref-3)
3. Clarification questionnaire available at :

<http://www.rohs.biois.eu/Ex_15-II_TI_Questionnaire-1_Clarification_Response.pdf> [↑](#footnote-ref-4)
4. Directive 2011/65/EU (RoHS) available at <http://eur-lex.europa.eu/LexUriServ/LexUriServ.do?uri=CELEX:32011L0065:EN:NOT> [↑](#footnote-ref-5)